WEST Search History

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DATE: Sunday, December 11, 2005

Hide?	Set Name	Query
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ
☐	L14	l5 and (clean$4 same (hf or hydrofluoric or (hydrogen fluoride)) same (peroxide or 'h.sub.2 'h.sub.2o.sub.2') same (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh
☐	L13	l5 and (clean$4 same (hf or hydrofluoric or (hydrogen fluoride)) same (peroxide or 'h.sub.2 'h.sub.2o.sub.2') same (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh
☐	L12	L11 and l5
☐	L11	high-k and (clean$4 same (hf or hydrofluoric or (hydrogen fluoride)) same (peroxide or 'h. 'h.sub.2o.sub.2') same (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh
☐	L10	high-k and ((hf or hydrofluoric or (hydrogen fluoride)) same (peroxide or 'h.sub.2 o.sub.2' 'h.sub.2o.sub.2') same (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh
☐	L9	L8 and (two near step)
☐	L8	L7 and clean$4
☐	L7	L6 and (residue or by-products or byproducts or conatminant$3)
☐	L6	high-k and ((hf or hydrofluoric or (hydrogen fluoride)) and (peroxide or 'h.sub.2 o.sub.2' o 'h.sub.2o.sub.2') and (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh')
☐	L5	("5782984"|"6043206"|"6132522"|"6171405"|"6192899"|"6277749"|"6399552"|"6486108"
☐	L4	20040026369
☐	L3	L2 and ((hf or hydrofluoric or (hydrogen fluoride)) and (peroxide or 'h.sub.2 o.sub.2' or 'h. and (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh'))
☐	L2	L1 and (etch$4 with (residue or by-products or byproducts or conatminant$3))
☐	L1	high-k dielectric

END OF SEARCH HISTORY

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DATE: Sunday, December 11, 2005

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		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ
☐	L11	high-k and (clean$4 same (hf or hydrofluoric or (hydrogen fluoride)) same (peroxide or 'h. 'h.sub.2o.sub.2') same (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh
☐	L10	high-k and ((hf or hydrofluoric or (hydrogen fluoride)) same (peroxide or 'h.sub.2 o.sub.2' 'h.sub.2o.sub.2') same (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh
☐	L9	L8 and (two near step)
☐	L8	L7 and clean$4
☐	L7	L6 and (residue or by-products or byproducts or conatminant$3)
☐	L6	high-k and ((hf or hydrofluoric or (hydrogen fluoride)) and (peroxide or 'h.sub.2 o.sub.2' o 'h.sub.2o.sub.2') and (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh')
☐	L5	("5782984"|"6043206"|"6132522"|"6171405"|"6192899"|"6277749"|"6399552"|"6486108"
☐	L4	20040026369
☐	L3	L2 and ((hf or hydrofluoric or (hydrogen fluoride)) and (peroxide or 'h.sub.2 o.sub.2' or 'h. and (ammonium or ammonia or 'nh.sub.3' or 'nh.sub.4 oh' or 'nh.sub.4oh'))
☐	L2	L1 and (etch$4 with (residue or by-products or byproducts or conatminant$3))
☐	L1	high-k dielectric

END OF SEARCH HISTORY

L11: Entry 33 of 57 File: PGPB Dec 25, 2003

DOCUMENT-IDENTIFIER: US 20030235947 A1
TITLE: METHOD FOR FABRICATING CAPACITOR IN SEMICONDUCTOR DEVICE

Summary of Invention Paragraph:
[0009] Therefore, it is a recent trend in increasing mainly the dielectric constant of the dielectric thin layer, and thus, obtaining the sufficient capacitance of the capacitor. A traditionally fabricated capacitor uses a silicon oxide layer or a silicon nitride layer as a source for the dielectric thin layer. However, it is more increasingly used in today a capacitor with a metal-insulator-poly si (hereinafter referred as to MIS) structure wherein it uses a high-k dielectric material, e.g., Ta.sub.2O.sub.5 as a dielectric thin layer.

Detail Description Paragraph:
[0026] Inside of the capacitor hole, a polysilicon layer for forming a lower electrode 24 is deposited till having a thickness in a range from about 100 .ANG. to about 500 .ANG., and a native oxide layer formed on the polysilicon layer is removed by cleaning a surface of the polysilicon layer with use of HF or a buffer oxide etchant (hereinafter referred as to BOE). At this time, it is possible to use NH.sub.4OH, H.sub.2O.sub.2 and H.sub.2O.sub.2 (SC-1) with a ratio of NH.sub.4OH:H.sub.2O.sub.2:H.sub- .2O.sub.2 is 1:4:20.

Detail Description Paragraph:
[0036] In continuous to the ALD process for forming the second dielectric thin layer 27, a third dielectric thin layer 28 is formed by depositing a Ta2O5 layer on the second dielectric thin layer 27 with a thickness ranging from about 30 .ANG. to about 100 .ANG.. At this time, a temperature and a pressure are maintained within a range from about 200.degree. C. to about 500.degree. C. and from about 0.1 Torr to about 1.0 Torr, respectively. Ta(C.sub.2H.sub.5O).sub.5 and O.sub.2 are especially used to form the Ta.sub.2O.sub.5 dielectric layer. Herein, O.sub.2 is used as a reactant gas. Also, the third dielectric thin layer 28 can use high-k dielectric materials such as (Ba,Sr)TiO.sub.3 or ferroelectric materials such as (pb,Zr) TiO.sub.3, (Pb,La)(Zr,Ti)O.sub.3, SrBi.sub.2Ta.sub.2O.sub.9, Bi.sub.4-xLa.sub.xTi.sub.3O.sub.12 and so forth.

L11: Entry 17 of 57 File: PGPB Mar 3, 2005

DOCUMENT-IDENTIFIER: US 20050048794 A1
TITLE: Method for making a semiconductor device having a high-k gate dielectric

Abstract Paragraph:
A method for making a semiconductor device is described. That method comprises forming a metal oxide layer on a substrate, converting at least part of the metal oxide layer to a metal layer; and oxidizing the metal layer to generate a metal oxide high-k gate dielectric layer.

Summary of Invention Paragraph:
[0001] The present invention relates to methods for making semiconductor devices, in particular, semiconductor devices that include high-k gate dielectric layers.

Summary of Invention Paragraph:
[0002] MOS field-effect transistors with very thin silicon dioxide based gate dielectrics may experience unacceptable gate leakage currents. Forming the gate dielectric from certain high-k dielectric materials, instead of silicon dioxide, can reduce gate leakage. Such a dielectric may not, however, be compatible with polysilicon--the preferred material for making the device's gate electrode.

Summary of Invention Paragraph:
[0003] When high-k films comprise an oxide formed using a metal halide precurser (e.g., a metal chloride), they may contain significant amounts of impurities (e.g., residual chlorine), which may adversely affect the electrical properties of a device that includes that film. In addition, an oxide based high-k film may manifest oxygen vacancies at random surface sites. When the device's gate electrode comprises polysilicon, a silicide may form where such vacancies occur. The silicide's presence may alter the electrode's workfunction or cause the device to short through the dielectric.

Summary of Invention Paragraph:
[0004] Accordingly, there is a need for an improved process for making a semiconductor device that includes a high-k gate dielectric. There is a need for such a process that forms a purified high-k film prior to forming a polysilicon gate electrode on that film. There is also a need for such a process that generates a high-k film with a nearly idealized metal:oxygen stoichiometry. The method of the present invention provides such a process.

Detail Description Paragraph:
[0006] A method for making a semiconductor device is described. That method comprises forming a metal oxide layer on a substrate, converting at least part of the metal oxide layer to a metal layer; and oxidizing the metal layer to generate a metal oxide high-k gate dielectric layer. In the following description, a number of details are set forth to provide a thorough understanding of the present invention. It will be apparent to those skilled in the art, however, that the invention may be practiced in many ways other than those expressly described here. The invention is thus not limited by the specific details disclosed below.

Detail Description Paragraph:
[0008] When the substrate comprises a silicon wafer, the wafer may be cleaned

before forming the metal oxide layer on its surface. To clean the wafer, it may initially be exposed to a dilute hydrofluoric acid ("HF") solution, e.g., a 50:1 water to HF solution. The wafer may then be placed in a megasonic tank, and exposed first to a water/H.sub.2O.sub.2/NH.sub.4- OH solution, then to a water/H.sub.2O.sub.2/HCl solution. The water/H.sub.2O.sub.2/NH.sub.4OH solution may remove particles and organic contaminants, and the water/H.sub.2O.sub.2/HCl solution may remove metallic contaminants.

Detail Description Paragraph:
[0011] As deposited, metal oxide layer 101 may include undesirable impurities, e.g., residual chlorine (represented by dots in FIG. 1a), which render that layer incompatible with polysilicon. The method of the present invention transforms metal oxide layer 101 into a metal oxide high-k gate dielectric layer that includes less impurities and that is compatible with polysilicon. A two step process induces that transformation. First, at least part of metal oxide layer 101 is converted into a metal layer. Second, that metal layer is oxidized to generate the metal oxide high-k gate dielectric layer.

Detail Description Paragraph:
[0017] Although the reduction operation will remove a significant amount of undesirable impurities (e.g., residual chlorine or another halogen--represented by dots in FIG. 1a) as part or all of metal oxide layer 101 is reduced to metal layer 102, FIG. 1b is not meant to suggest that this reduction step will remove all undesirable impurities, which were initially present in metal oxide layer 101. That process step may, however, remove a sufficient number of those impurities to ensure that a subsequently formed metal oxide high-k gate dielectric layer will be compatible with a gate electrode to be formed on it. Thus, a method that removes a significant number of the undesirable impurities initially present in metal oxide layer 101, but which does not remove all--or even substantially all--of those impurities, still falls within the spirit and scope of the present invention.

Detail Description Paragraph:
[0020] After metal oxide layer 101 has been reduced to metal layer 102, metal layer 102 is oxidized, e.g., by using an oxidizing agent. That oxidizing agent may comprise a solution that contains a mild oxidant, such as a peroxide (e.g., hydrogen peroxide or an organic peroxide) or ozone. Alternatively, the oxidizing agent may comprise an oxidizing gas, e.g., one that contains oxygen. Such an oxidation step may convert metal layer 102 into metal oxide high-k gate dielectric layer 103, as shown in FIG. 1c.

Detail Description Paragraph:
[0021] The resulting metal oxide high-k gate dielectric layer 103 will comprise a material with a dielectric constant that is greater than the dielectric constant of silicon dioxide, and that preferably is at least about twice that of silicon dioxide, i.e., a dielectric constant that is greater than about 8. A mild oxidation process (i.e., a more controllable and less aggressive procedure) should be used to prevent oxidation of substrate 100, or to at least minimize the amount of substrate oxidation. Preferably, no oxidation occurs on the substrate, when the metal layer is oxidized to generate the metal oxide high-k gate dielectric layer. In some cases, however, an insignificant amount of oxidation, e.g., less than about 10 angstroms (equal to 1 or 2 monolayers), may grow on substrate 100 without adversely affecting the overall process.

Detail Description Paragraph:
[0025] Although a few examples of processes for oxidizing metal layer 102 are described here, other oxidizing treatments may be used, as will be apparent to those skilled in the art. Examples include other types of chemical oxidation processes, e.g., those using aqueous solutions with different oxidizing agents. A plasma assisted oxidation process may be used, as may various combinations of these processes. The process used to oxidize metal layer 101 is thus not limited to those

described above. The method of the present invention contemplates using any suitable oxidizing step that takes place in any suitable oxidizing ambient, or any acceptable chemical treatment that serves to replace the oxygen that was removed by the preceding reduction step. In a preferred embodiment, the amount of oxygen included in metal oxide high-k gate dielectric layer 103 significantly exceeds the amount of oxygen included in metal oxide layer 101.

Detail Description Paragraph:
[0026] Following the oxidation of metal layer 102 to form metal oxide high-k gate dielectric layer 103, a gate electrode may be formed directly on dielectric layer 103. In a preferred embodiment, the gate electrode may be formed by initially depositing polysilicon layer 104 on dielectric layer 103--generating the FIG. 1d structure. Polysilicon layer 104 may be deposited using conventional methods and preferably is between about 500 angstroms and about 4,000 angstroms thick. After etching both layers 104 and 103 to form the FIG. 1e structure, additional steps that are generally used to complete the gate electrode (e.g., forming a silicide (not shown) on the upper part of etched polysilicon structure 105) may be applied. As such steps are well known to those skilled in the art, they will not be described in more detail here. Although the gate electrode preferably comprises polysilicon, it may alternatively be formed from various metals with which metal oxide high-k gate dielectrics may be used. In addition, the gate electrode may comprise a combination of polysilicon and one or more metal or semi-metal materials.

Detail Description Paragraph:
[0027] As described above, reducing all or part of a metal oxide layer to form a metal layer, then reoxidizing that metal layer may yield a purified metal oxide high-k gate dielectric layer. Such a purified dielectric layer may include less than about twenty percent (20%) of the impurities that were included in the metal oxide layer. In addition, reoxidizing the metal layer using a mild oxidation process may generate a metal oxide high-k gate dielectric layer with a nearly idealized metal:oxygen stoichiometry, without causing a significant amount of oxide to form on the underlying substrate. As a consequence, the resulting metal oxide high-k gate dielectric layer may be used with a polysilicon-based gate electrode.

Detail Description Paragraph:
[0028] Although the embodiments described above are examples of processes for transforming a metal oxide layer into a metal oxide high-k gate dielectric layer that includes substantially less impurities and an improved metal:oxygen stoichiometry, the present invention is not limited to these particular embodiments. The present invention contemplates other processes that transform a metal oxide layer into a metal oxide high-k gate dielectric layer that is compatible with a gate electrode to be formed on it.

Detail Description Paragraph:
[0029] In the method of the present invention, a single reduction/reoxidation sequence may be applied after forming metal oxide layer 101. Alternatively, an iterative approach may be applied, e.g., when a relatively thick film is desired. In such an iterative process, a series of metal oxide deposition steps alternate with the above described reduction/reoxidation steps. After the initial metal oxide high-k gate dielectric layer is generated, a second metal oxide layer is formed on its surface. A second metal oxide high-k gate dielectric layer is then formed by reducing the second metal oxide layer to a second metal layer, then oxidizing that second metal layer. A third metal oxide layer may then be formed followed by a third reduction/reoxidation sequence, and so on, until the desired thickness for the metal oxide high-k gate dielectric layer is achieved.

Detail Description Paragraph:
[0030] Although the foregoing description has specified certain steps and materials that may be used in the method of the present invention, those skilled in the art

will appreciate that many modifications and substitutions may be made. For example, although the gate electrode preferably is formed directly on the metal oxide high-k gate dielectric layer, intermediary layers may be formed between the dielectric layer and the gate electrode. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the invention as defined by the appended claims.

CLAIMS:

1. A method for making a semiconductor device comprising: forming a metal oxide layer on a substrate; converting at least part of the metal oxide layer to a metal layer; and oxidizing the metal layer to generate a metal oxide high-k gate dielectric layer.

3. The method of claim 2 further comprising forming a gate electrode on the metal oxide high-k gate dielectric layer and wherein the metal oxide high-k gate dielectric layer comprises a material selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide.

9. The method of claim 1 wherein the metal layer is oxidized to generate a metal oxide high-k gate dielectric layer by exposing the metal layer to an oxidizing agent.

12. A method for making a semiconductor device comprising: forming a metal oxide layer on a substrate, the metal oxide layer comprising halide impurities and a material selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide; reducing at least part of the metal oxide layer to a metal layer by exposing the metal oxide layer to hydrogen; oxidizing the metal layer to generate a metal oxide high-k gate dielectric layer; and forming a polysilicon based gate electrode on the metal oxide high-k gate dielectric layer.

14. The method of claim 12 wherein the metal layer is oxidized to generate a metal oxide high-k gate dielectric layer by exposing the metal layer to a solution that contains a peroxide.

15. The method of claim 12 wherein the metal layer is oxidized to generate a metal oxide high-k gate dielectric layer by exposing the metal layer to a gas that contains oxygen.

16. The method of claim 12 wherein the amount of halide impurities included in the metal oxide high-k gate dielectric layer is less than about twenty percent of the amount of halide impurities included in the metal oxide layer, and the amount of oxygen included in the metal oxide high-k gate dielectric layer exceeds the amount of oxygen included in the metal oxide layer.

17. The method of claim 12 wherein no oxidation occurs on the substrate, when the metal layer is oxidized to generate a metal oxide high-k gate dielectric layer.

18. A method for making a semiconductor device comprising: forming a metal oxide layer on a substrate, the metal oxide layer comprising halide impurities and a material selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide; reducing substantially all of the metal oxide layer to a metal layer by exposing the metal oxide layer to a hydrogen containing gas: oxidizing the metal layer to generate a metal oxide high-k gate dielectric layer by exposing the metal layer to a solution that comprises a compound selected from the group consisting of hydrogen peroxide, an organic peroxide, and ozone or by exposing the metal layer to a gas that contains oxygen; and forming a polysilicon based gate electrode on the metal oxide high-k gate dielectric layer; wherein the amount of halide impurities included in the metal oxide high-k gate dielectric layer is substantially less than the amount of halide impurities

included in the metal oxide layer, and the amount of oxygen included in the metal oxide high-k gate dielectric layer significantly exceeds the amount of oxygen included in the metal oxide layer.

19. The method of claim 18 wherein an insignificant amount of oxidation occurs on the substrate, when the metal layer is oxidized to generate a metal oxide high-k gate dielectric layer.

20. The method of claim 19 wherein less than about 10 angstroms of oxide grows on the substrate, when the metal layer is oxidized to generate a metal oxide high-k gate dielectric layer.

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L11: Entry 16 of 57 File: PGPB Mar 31, 2005

DOCUMENT-IDENTIFIER: US 20050070120 A1
TITLE: Methods and devices for an insulated dielectric interface between high-k material and silicon

Abstract Paragraph:
Methods and devices are described for an insulated dielectric interface between a high-k material and silicon for improving electrical characteristics of devices. A method includes forming an oxide layer on a silicon substrate using an in situ steam generation process, etching the oxide layer to form a reduced thickness oxide layer of less than 10 Angstroms, and annealing the reduced thickness oxide layer with ammonia. A semiconductor wafer comprises a silicon substrate, an oxide layer coupled to the silicon substrate where the oxide layer having a thickness of less than 10 Angstroms, and a high-k dielectric material deposited onto the oxide layer.

Cross Reference to Related Applications Paragraph:
[0001] This patent application claims priority to, and incorporates by reference in its entirety, U.S. provisional patent application Ser. No. 60/498,676 filed on Aug. 28, 2003, entitled, "A Method for Forming an Insulated Dielectric Interface Between High-K Material and Silicon."

Summary of Invention Paragraph:
[0003] The present invention relates generally to semiconductor devices. More particularly, it concerns formation of a thin insulator dielectric interface between high-k material and silicon on a semiconductor device.

Summary of Invention Paragraph:
[0005] As research and development of dielectric materials advances, especially materials where the dielectric constant, k, is greater than 3.9, an insulator dielectric interface layer between a high-k film and a silicon substrate has proven beneficial. For example, the insulator dielectric interface layer may improve device electrical characteristics including leaking current density, mobility, transconductance and the saturated current.

Summary of Invention Paragraph:
[0010] According to another aspect of the invention, a method comprises: forming an oxide layer on a silicon substrate using an in situ steam generation process, etching the oxide layer to form a reduce thickness oxide layer of approximately less than 10 Angstroms, annealing the reduced thickness oxide layer, and depositing a high-k dielectric material on the reduced thickness oxide layer.

Summary of Invention Paragraph:
[0011] According to yet another aspect of the invention, a semiconductor wafer is disclosed. The semiconductor wafer includes a silicon substrate, an oxide layer coupled to the silicon substrate, where the oxide layer is formed from an in situ steam generation process and etched back to a thickness of approximately 10 Angstroms, and a high-k dielectric material deposited on the oxide layer.

Summary of Invention Paragraph:
[0012] Further, the invention includes a semiconductor wafer which includes a

silicon substrate, an oxide layer coupled to the silicon substrate, where the oxide layer is formed from an in situ steam generation process and etched back to a thickness of approximately 4 Angstroms, and a high-k dielectric material deposited on the oxide layer.

Detail Description Paragraph:
[0027] The invention sets forth methods and devices for a thick insulator dielectric at an interface and reducing the thickness by a controlled etch back. In particular, the invention is directed toward scaling down the equivalent oxide thickness and applying a NH.sub.3 anneal process prior to the deposition of a high-k dielectric film, in which k may be greater than 3.9. This prevents further oxide growth in subsequent fabrication steps and reduces the equivalent oxide thickness. The equivalent oxide thickness ("EOT"), as described herein, relates to the performance of a metal on silicon (MOS) gate dielectric, where the dielectric constant, k, is about 3.9, and where the MOS gate may include a high-k material. The treated oxide layer has been found to be beneficial in improving device electrical characteristics, including leakage current density, mobility, transconductance and saturated current, I.sub.dsat.

Detail Description Paragraph:
[0030] Alternatively, in other embodiments, a chemical oxide layer is formed on a silicon wafer using an RCA-type cleaning method which may include a HF/HCl--SCl--SC2 sequence. The HF/HCl etch portion such as a 200:1:0.4 DI:HF:HCl formula at 23.degree. C. may be dispensed and targeted to remove a thickness of the oxide. SC1 may be dispensed onto the wafer at a particular temperature and duration, e.g., 23.degree. C. for 7 minutes, with a H.sub.2O:H.sub.2O.sub.2:NH.sub.4OH mixture with the ratio of 100:2:1, respectively. Finally, SC2 may be dispensed onto the wafer at a predetermined temperature and duration, e.g., 23.degree. C. for 7 minutes with a H.sub.2O:H.sub.2O.sub.2:HCl mixture of 50:1:1, respectively. After the SC2 rinse, the wafers may be transferred to the LPD where they received a 3-minute DI water rinse and a low pressure isopropyl alcohol/hot N.sub.2 dry.

Detail Description Paragraph:
[0033] For each embodiment described above, the wafers undergo an ammonia (NH.sub.3) anneal process at 700.degree. C. and 30 Torr for 15 seconds prior to the deposition of a high-k material. The anneal process, in conjunction with the scaling of the oxide interfaces, achieves thinner EOTs with acceptable electrical performances. Referring to FIG. 3, annealed oxide layer 30 is the result of an etching step (e.g., chemical etch, vapor etch, etc.) and the annealing process. Annealed oxide layer 30 may be less than or equal to approximately 10 .ANG.. More precisely, oxide layer 30 may be less than or equal to approximately 4 .ANG.. Even more precisely, oxide layer 30 may be less than or equal to approximately 3.7 .ANG..

Detail Description Paragraph:
[0034] Referring to FIG. 4, following the annealing process, a high-k dielectric material 32 may be deposited on annealed oxide layer 30. The high-k dielectric material may be ZrO.sub.2, Zr silicate, ZrSiON, Hf silicate, HfO.sub.2, HfSiON, HfON, Hf-Aluminates, AlZrO.sub.2, AlZrSiO.sub.2, AlHfSiO.sub.2, Al.sub.2l O.sub.3, La2O.sub.3, La silicate, Y.sub.2O.sub.3, Y silicate, LaAlO.sub.3, Gd.sub.2O.sub.2, Gd silicate, Pr.sub.3O.sub.2, Pr silicate, or any of their hybrid combinations including nitrogen bearing high-k films. In one embodiment, the high-k dielectric material is HfSi.sub.xO.sub.y film of approximately 45 .ANG. deposited on annealed oxide layer 30. Following the high-k dielectric material deposition, a post high-k ammonia anneal process may be performed at 700.degree. C. and 30 Torr for 60 seconds.

Detail Description Paragraph:
[0054] Next, a high-k deposition process consisted of an HfSi.sub.xO.sub.y film was deposited on all the wafers at 4 Torr, 485.degree. C., and 45 .ANG.. The wafers

were then treated with a post high-k dielectric deposition. This was an NH.sub.3 anneal at 700.degree. C. and 30 Torr for 60 seconds. The deposition and post-treatment were completed as part of a sequenced recipe on a RTP.

Detail Description Paragraph:
[0061] Referring to FIGS. 6A-6C, a list of results of the oxide formed from the above embodiments and the respective EOT. Column 1 lists the 25 different wafers fabricated and tested. Column 2, entitled "Clean/Interface" refers to the cleaning and formation of the different types of oxide. Column 3, entitled "Interface Thickness (.ANG.)" refers to the thickness of the oxide after the etching and ammonia annealing process. Column 4, entitled "Avg. Interface Thickness (.ANG.)" is an average thickness of all the wafers that have the same cleaning and formation process. Column 5, entitled "RTP01 Pre-Treatment" lists which wafer received the ammonia anneal process prior to the deposition of the high-k dielectric material deposition. Column 6, entitled "High-k Films" is the type and film deposited on the oxide layer. Column 7, entitled "Post High-k Treatment" is the ammonia anneal process done after the deposition of the high-k dielectric material. Column 8, entitled "Electrode" is the type of silicon substrate interface in which the oxide layer is formed. Column 9, entitled "EOT (.ANG.)" is the equivalent oxide thickness for the respective semiconductor device on the wafer. Column 10, entitled "AVG EOT (.ANG.)" is the average of the wafers in each experimental split (e.g. wafers 2, 3, 4 are one split, wafers 5, 6 are another split, etc.). Column 11-16 are electrical tests done on the transistors formed on the respective wafer.

Detail Description Paragraph:
[0066] To further illustrate the effect of the starting interface, the thickness of the starting interface was plotted against the contribution of the high-k and subsequent processing effects, calculated for each split as interface thickness subtracted from the EOT, as shown in FIG. 8. Since all wafers had the same 45 .ANG. thick HfSi.sub.xO.sub.y film, subsequent processing after high-k deposition may have caused additional contributions due to growth or changes in composition of the interfacial oxide. The changes in the composition could possibly be caused by diffusion of the HfSi.sub.xO.sub.y into the interface. Based on these assumptions, it appears that the thicker the starting interfacial layer, the less additional growth or fewer compositional changes. Additionally, it appears that the NH.sub.3 pre-treatment helped suppress additional changes; the thinner the initial interface, the greater the suppression.

Detail Description Paragraph:
[0076] FIG. 14 shows the effective mobility curves generated from a mobility model for each split. The mobilities were all low, as had been seen with all high-k films studied to date. For high-k films, the data point of interest was the mobility at a high field value of 1.3E+6 V/cm. To differentiate between the clean/pre-treatment splits of interest, the median value of each split was plotted against the EOT. The resultant graph, FIG. 15 shows that the high field mobility values reduced as EOT reduced.

Detail Description Table CWU:
1TABLE 1 Recipe an IMEC type-clean STEP 1 2 3 4 5 6 7 8 TIME (seconds) 60 120 628 120 600 35 270 30 de-ionized water DIW .cndot. .cndot. .cndot. .cndot. .cndot. DIW-1 O3 .cndot. NH.sub.4OH H.sub.2O.sub.2 HF .cndot. Lo-flow HCL .cndot. .cndot. High-flow HCL SH .cndot. QDR .cndot. DIP .cndot. DSM .cndot. DIW-H DSM-PW 6

CLAIMS:

8. The method of claim 1, further comprising, depositing a high-k dielectric material on the reduced thickness oxide layer.

9. The method of claim 8, the high-k dielectric material comprising ZrO.sub.2, Zr silicate, ZrSiON, Hf silicate, HfO.sub.2, HfSiON, HFON, Hf-Aluminates, AlZrO.sub.2,

AlZrSiO.sub.2, AlHfSiO.sub.2, Al.sub.2O.sub.3, La2O.sub.3, La silicate, Y.sub.2O.sub.3, Y silicate, LaAlO.sub.3, Gd.sub.2O.sub.3, Gd silicate, Pr.sub.3O.sub.2, Pr silicate, or any combination thereof.

10. The method of claim 9, the high-k dielectric comprising HfSi.sub.xO.sub.y film having a thickness of approximately 20 to 45 Angstroms.

11. The method of claim 8, further comprising after depositing the high-k dielectric material, annealing the silicon substrate at approximately 700.degree. C. at 30 Torr for a predetermined time.

12. A method comprising: providing a silicon substrate; forming an oxide layer on the silicon substrate using an in situ steam generation process; etching the oxide layer to form a reduced thickness oxide layer of less than approximately 10 Angstroms; annealing the reduced thickness oxide layer; and depositing a high-k dielectric material on the reduce thickness oxide layer.

15. The method of claim 12, the high-k dielectric material having a thickness of approximately 45 Angstroms.

16. The method of claim 12, the high-k dielectric material comprising ZrO.sub.2, Zr silicate, ZrSiON, Hf silicate, HfO.sub.2, HfSiON, HfON, Hf-Aluminates, AlZrO.sub.2, AlZrSiO.sub.2, AlHfSiO.sub.2, Al.sub.2O.sub.3, La2O.sub.3, La silicate, Y.sub.2O.sub.3, Y silicate, LaAlO.sub.3, Gd.sub.2O.sub.3, Gd silicate Pr.sub.3O.sub.2, Pr silicate, or any combination thereof.

17. The method of claim 16, the high-k dielectric material comprising an HfSi.sub.xO.sub.y film.

18. A semiconductor wafer comprising: a silicon substrate; an oxide layer coupled to the silicon substrate, the oxide layer being formed from an in situ steam generation process and etched back to a thickness of less than 10 Angstrom; a high-k dielectric material coupled to the oxide layer.

20. The semiconductor wafer of claim 18, the high-k dielectric material having a thickness of approximately 45 Angstroms.

21. A semiconductor wafer comprising: a silicon substrate; an oxide layer coupled to the silicon substrate, the oxide layer formed from an in situ steam generation process and etched back to a thickness of less than 4 Angstrom; a high-k dielectric material coupled to the oxide layer.

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L11: Entry 13 of 57 File: PGPB Jun 2, 2005

DOCUMENT-IDENTIFIER: US 20050116266 A1
TITLE: Method of producing insulator thin film, insulator thin film, method of manufacturing semiconductor device, and semiconductor device

Summary of Invention Paragraph:
[0005] However, in the process of manufacturing a transistor using an electrode of polysilicon (poly-Si) which is currently used for silicon oxide, an activation annealing at a temperature of 1000.degree. C. or above is required. However, the high dielectric constant films (also called high-k films) of ZrO.sub.2, HfO.sub.2 and the like are low in heat resistance, are liable to undergo crystallization, and are liable to undergo a siliciding reaction with the silicon (Si) substrate, with the result of an increase in the leak current. In an attempt to solve these problems, it has been known that the heat resistance can be enhanced and the leak current can be reduced by using Hf(Zr)SiO or Hf(Zr)SiON to which silicon (Si) and nitrogen (N) have been added (see, for example, Japanese Patent Laid-open No. 2000-58832).

Summary of Invention Paragraph:
[0006] A problem to be solved lies in that, in the case of forming a high-k film according to the related art, immobile electric charges are generated at the boundaries between the high-k film and the Si substrate and the poly-Si electrode, resulting in a shift of threshold voltage (Vth) and mobility degradation. Another problem to be solved lies in that, in PMOS transistors, boron with which the gate electrode is doped would, upon the subsequent heat treatment, punch through the high dielectric constant film so as to diffuse to the substrate side. It has been known that the punch-through of boron can be restrained by the addition of nitrogen. However, in the case where nitrogen is added according to the related art, nitrogen would enter into the substrate, thereby increasing the interface level.

Detail Description Paragraph:
[0028] The surface of the substrate 100 is cleaned. The cleaning is conducted by using, for example, a solution prepared by mixing ammonia, hydrogen peroxide solution and pure water so as to decontaminate the surface of the substrate 100. Subsequently, a spontaneous oxide film on the surface of the substrate 100 is removed, for example, by immersing the substrate 100 in an aqueous hydrofluoric acid solution having an HF/H.sub.2O ratio of 1/100.

L11: Entry 23 of 57 File: PGPB Sep 9, 2004

DOCUMENT-IDENTIFIER: US 20040173812 A1
TITLE: Shallow trench isolation process

Detail Description Paragraph:
[0055] Referring to FIG. 6, in some embodiments, trench structure 55 may include a secondary protective liner 78 formed proximate first dielectric layer 72. This protective liner 78, preferably a dielectric material such as silicon nitride or silicon dioxide, may be deposited conformally over first dielectric layer 72. Protective liner 78 may have a thickness T.sub.6 of, e.g., 50-500 .ANG.. Because in some embodiments first dielectric layer 72 may contain Ge, it may be susceptible to attack by etchants used during subsequent processing, e.g., wet cleans such as hydrofluoric acid or even rinses in deionized water. Protective liner 78 may be selected to have a lower etch rate than first dielectric layer 72 in wet etchants such as hydrofluoric acid, or an RCA SC1 clean including water, hydrogen peroxide, and ammonium hydroxide. The formation of the secondary protective liner 78 may thus help to protect first dielectric layer 72 from accelerated etching, thereby preserving the integrity of first dielectric layer 72 during subsequent process steps. Protective liner 78 may also protect the sidewalls of trench 50 from oxidation during subsequent process steps performed at elevated temperatures and/or in ambients containing oxygen. The volume expansion from such oxidation may result in unwanted compressive strain being induced in the region bounded by the trench structure or in the channel region of subsequently fabricated devices.

Detail Description Paragraph:
[0067] Source and drain regions 102, 104 may be formed by, e.g., ion implantation of either n-type or p-type dopants. Gate 110 may be formed of a conductive material, such as doped semiconductor, e.g., polycrystalline Si or polycrystalline SiGe; a metal, e.g., titanium (Ti), tungsten (W), molybdenum (Mo), tantalum (Ta), nickel (Ni), or iridium (Ir); or metallic compounds, e.g., titanium nitride (TiN), titanium silicon nitride (TiSiN), tungsten nitride (WN), tantalum nitride (TaN), tantalum silicide (TaSi), nickel silicide (NiSi), or iridium oxide (IrO.sub.2), that provide an appropriate workfunction. The gate dielectric layer 114 may be formed on strained layer 18 by, for example, growing a SiO.sub.2 layer by thermal oxidation. Alternatively, gate dielectric layer 114 may include a high-k material with a dielectric constant higher than that of SiO.sub.2, such as ZrO.sub.2, Al.sub.2O.sub.3, HfO.sub.2, HfSiON, or HfSiO.sub.4. In some embodiments, gate dielectric layer 114 may be a stacked structure, e.g., a thin SiO.sub.2 layer capped with a high-k material.

L11: Entry 30 of 57 File: PGPB Feb 26, 2004

DOCUMENT-IDENTIFIER: US 20040038436 A1
TITLE: Method of manufacturing a semiconductor integrated circuit device

Detail Description Paragraph:
[0054] Subsequently, in a cleaning step for removing the foreign matters and contaminants in the etching step, a wet cleaning using a solution is performed. As the solution, a NH.sub.4OH/H.sub.2O.sub.2 or HCl/H.sub.2O.sub.2 aqueous solution, or a HF solution is used. The solution is used by adjusting the mixing ratio, time, solution temperature, and the like according to the type of generated contamination. The HF solution to be used is capable of selectively removing a hard mask of SiO type with respect to Si.

Detail Description Paragraph:
[0072] In Embodiments 1 and 2, there were respectively shown the cases in each of which a silicon dioxide film (SiO.sub.2 film) was used as the gate insulating film. However, when an Al.sub.2O.sub.3 film, a Ta.sub.2O.sub.5 film, an oxinitride film, or a high dielectric film (high-k material) is adopted, it is possible to perform trimming by either of the methods of Embodiments 1 and 2.

Detail Description Paragraph:
[0085] Below, a description will be given to an embodiment in which a transistor of a High-K (insulating film)/metal gate structure is formed. In this embodiment, the method of the present invention is applied to a damascene gate utilizing a dummy gate.

Detail Description Paragraph:
[0088] Subsequently, cleaning is performed with a NH.sub.4OH/H.sub.2O.sub.- 2 or HCl/H.sub.2O.sub.2 aqueous solution, or a HF solution to remove foreign matters and metal contaminants. Then, a stopper layer 408 and TEOS (hard mask) 403 made up of an oxide film are removed.

Detail Description Paragraph:
[0092] After the cleaning step, a high-k material 413 made of Ta.sub.2O.sub.5, Al.sub.2O.sub.3, and SiN is deposited, and a metal gate electrode material 412 such as W is deposited thereon (FIG. 4D). Thereafter, the metal gate electrode material 412 is etched to form a T-type metal gate 417.